

FIGURE 1

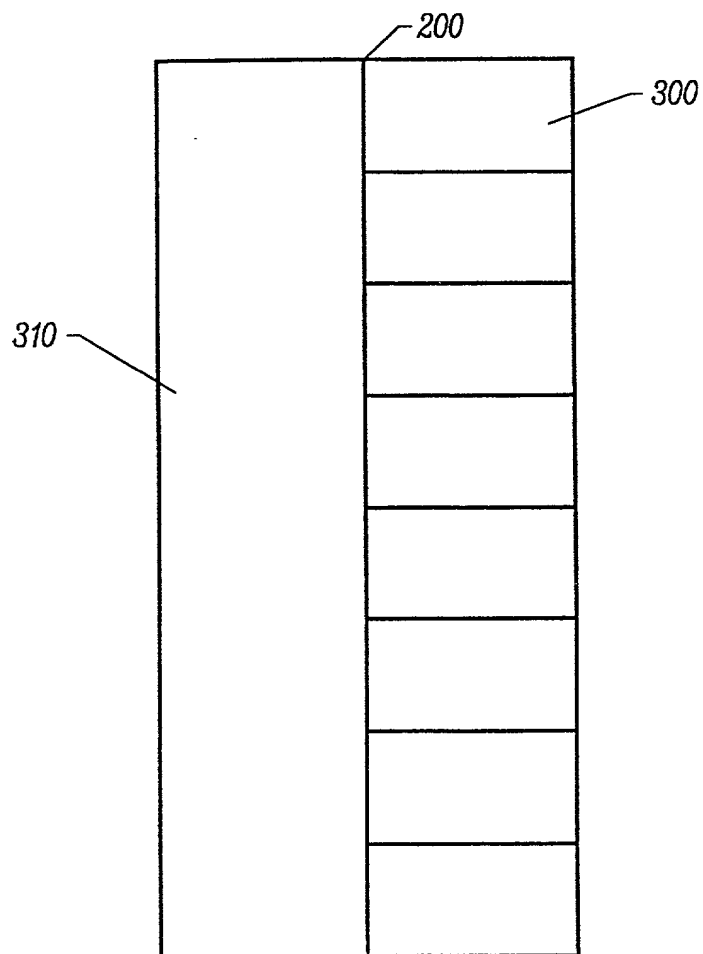
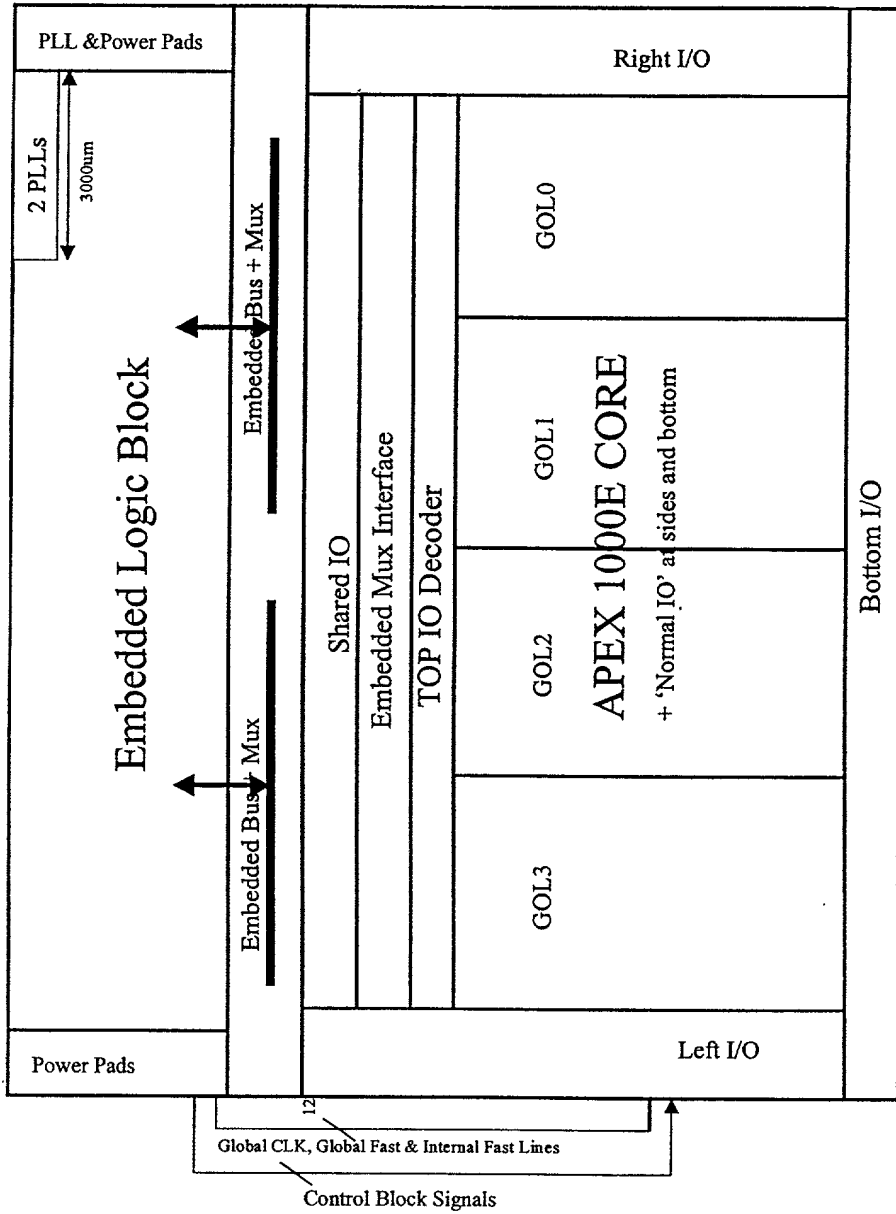


FIGURE 4



Top Level Floorplan

FIGURE 2

Patented by the U.S. Patent and Trademark Office

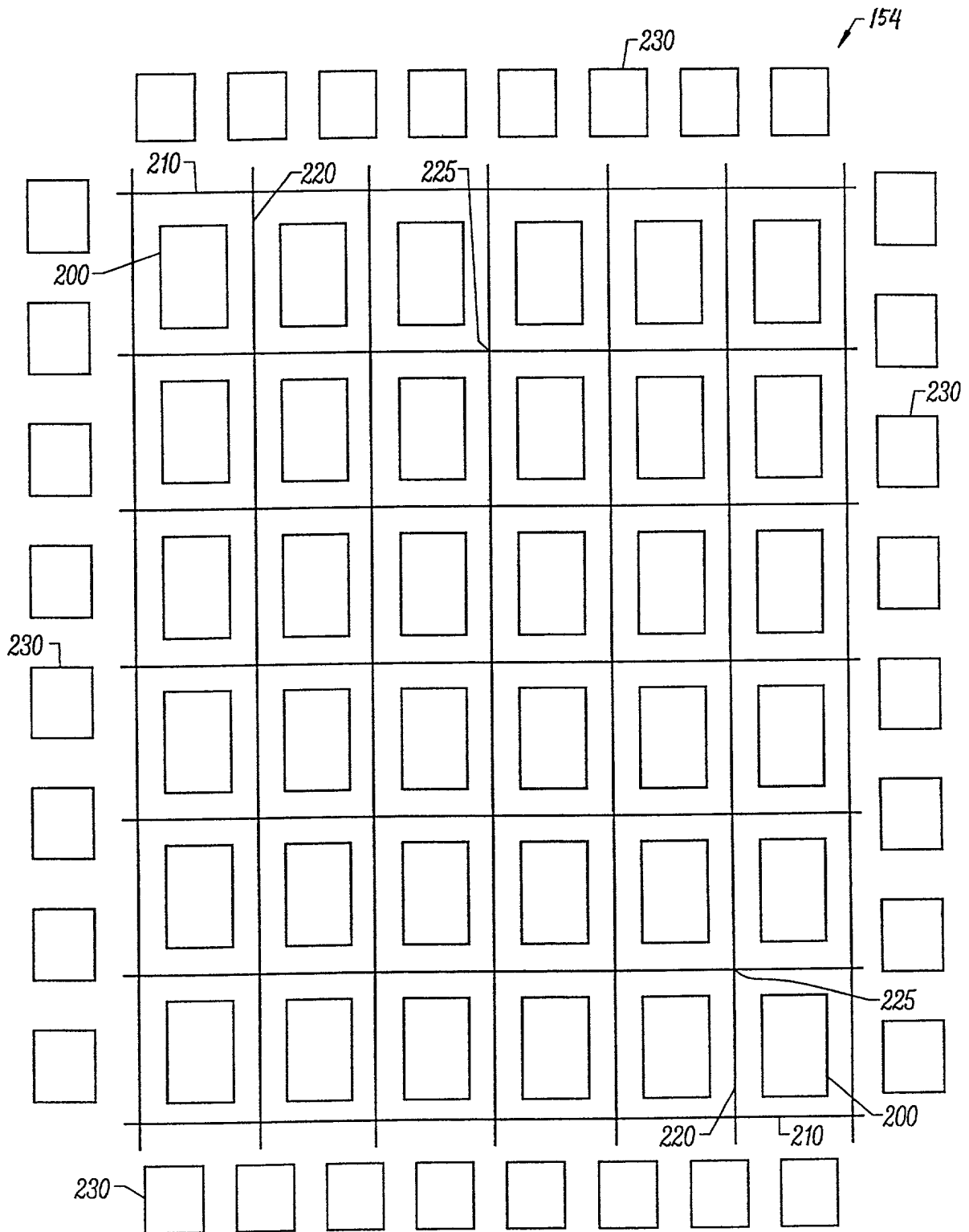


FIGURE 3

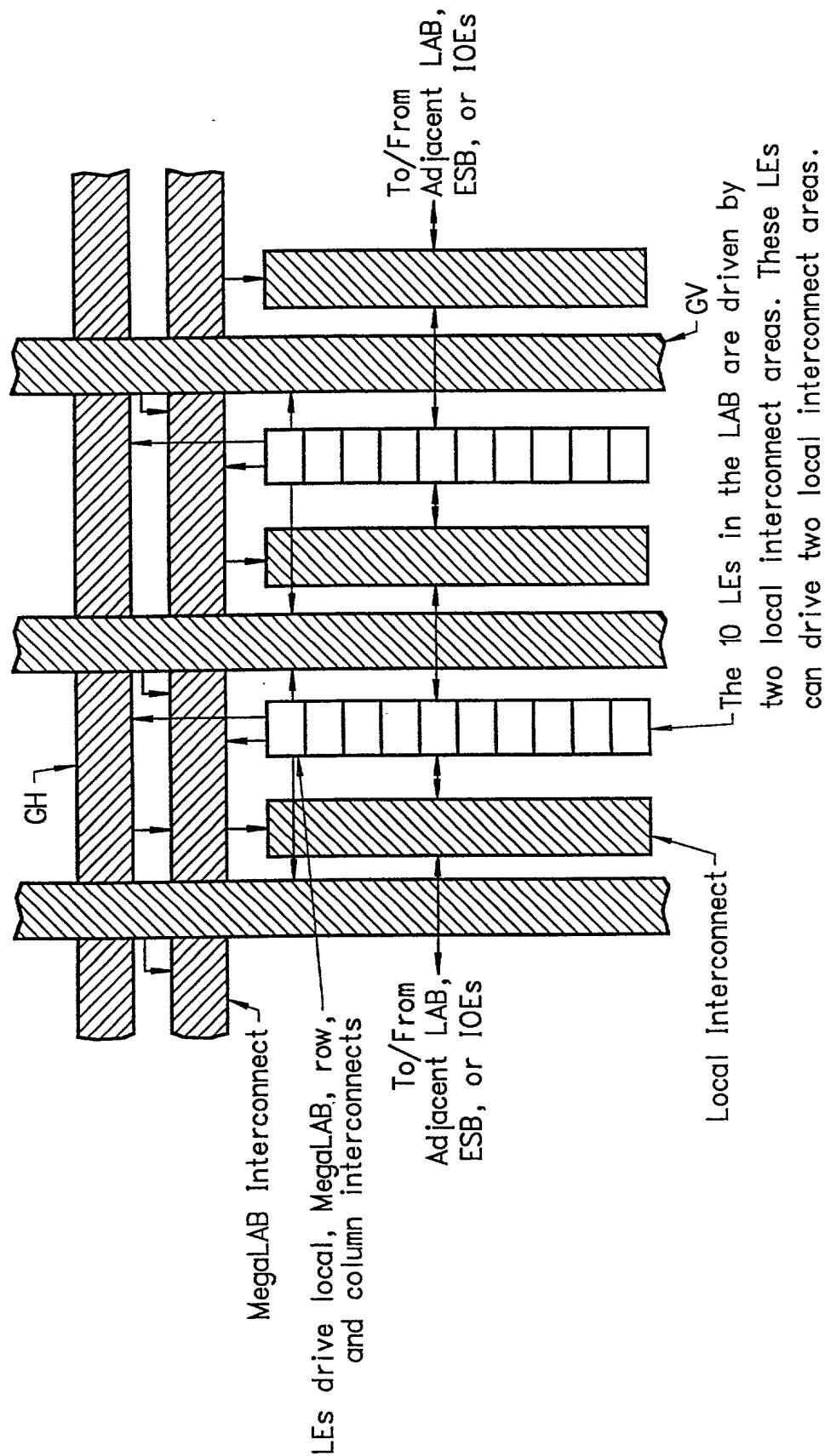


FIGURE 6

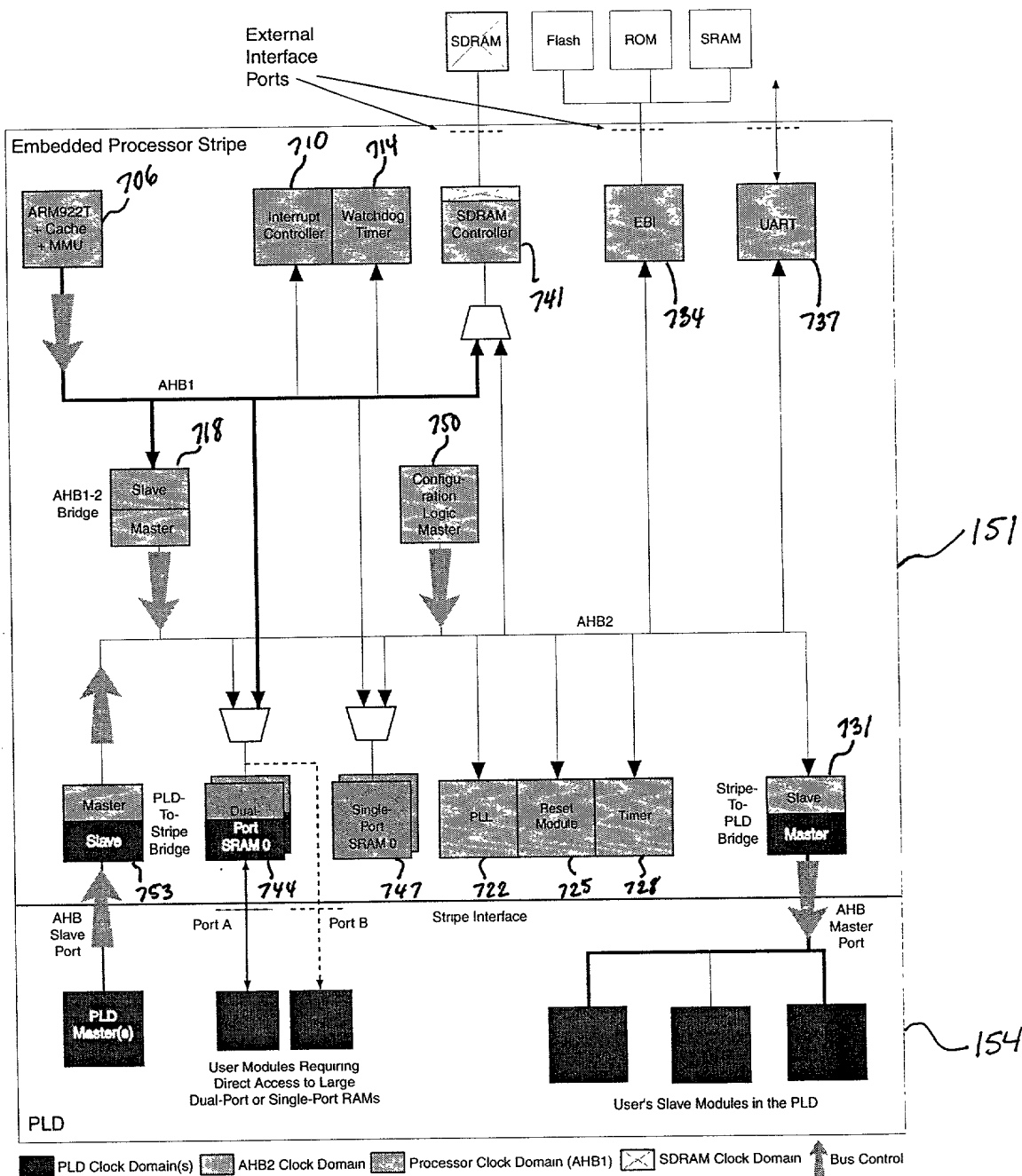


FIGURE 7

FIGURE 8

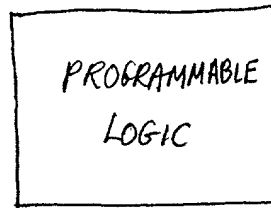


FIGURE 9

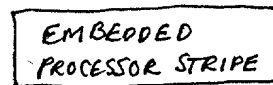


FIGURE 10

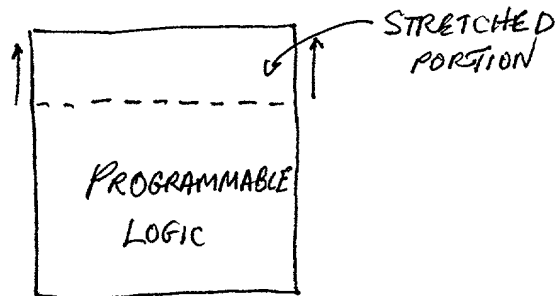
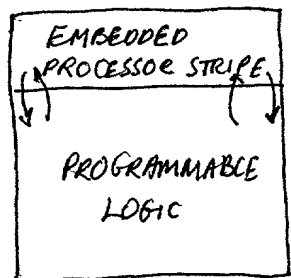


FIGURE 11



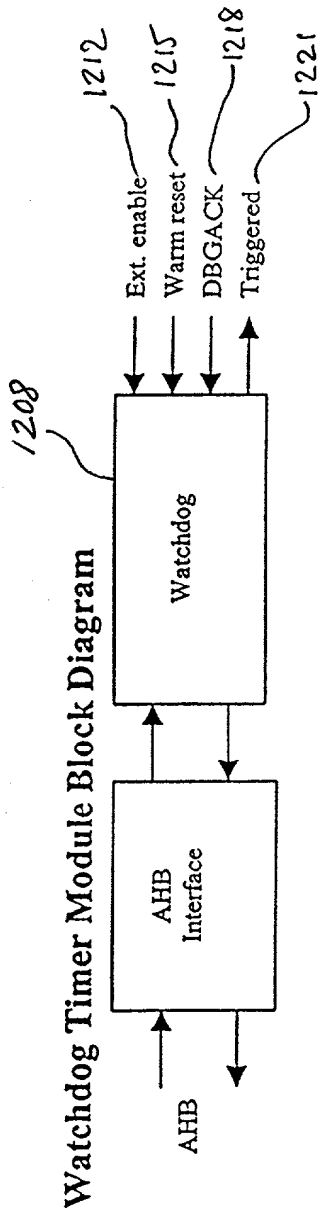


FIGURE 12

Control Register (WDOG_CR) – Read/Write

Register : WDOG_CR										Address : Address Base + 0x4C0										Access: Read/Write											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										TRIGGER										0										LK	

- LK R/W When this bit has the value 1 further writes to the register have no effect.
- TRIGGER R/W 0 means watchdog disabled. Other values specify bits 29:4 of the trigger value (bits 3:0 of the trigger are always zero).
- 0 R Reserved for future use. Write as 0 to ensure future compatibility.

FIGURE 13

Register: WDOG_COUNT
Address: Address Base + 0x4C4
Access: Read

COUNT	
31	
30	
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

FIGURE 14

Register: WDOG_RELOAD	Address: Address Base + 0x4C8	Access: Write
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[illegible]

FIGURE 15

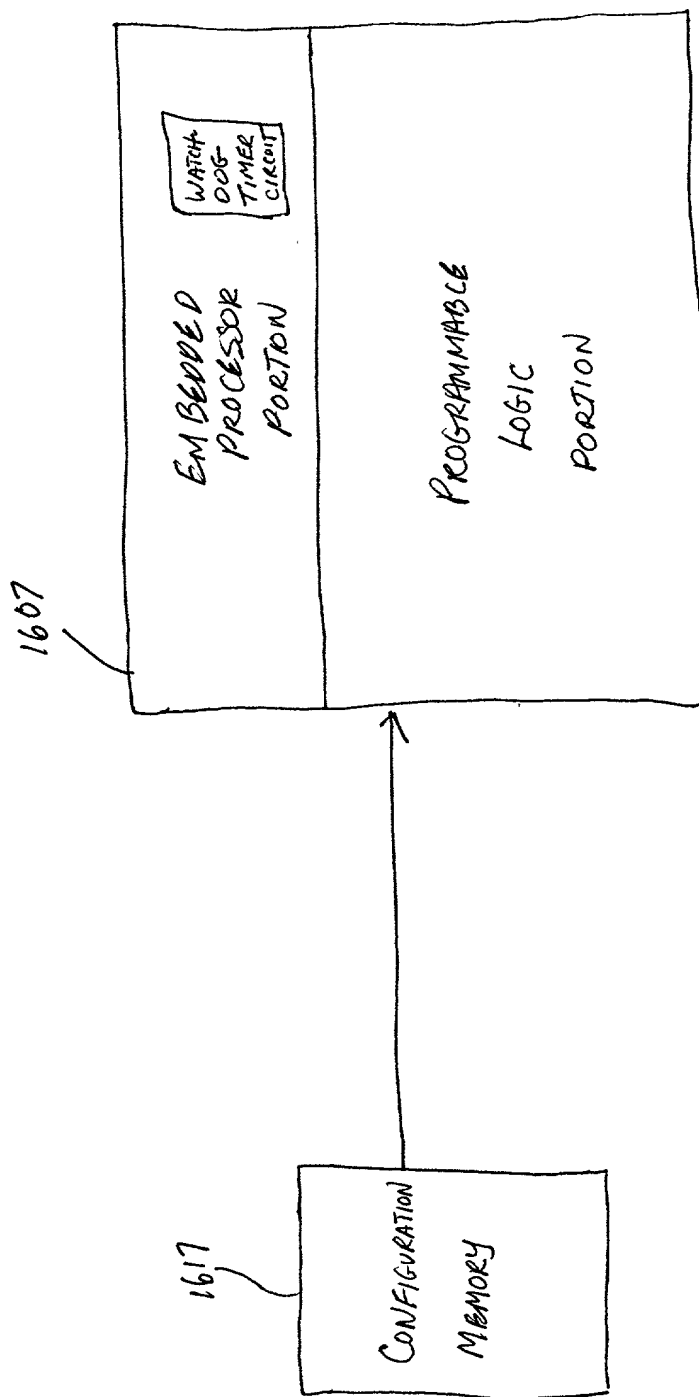


FIGURE 16

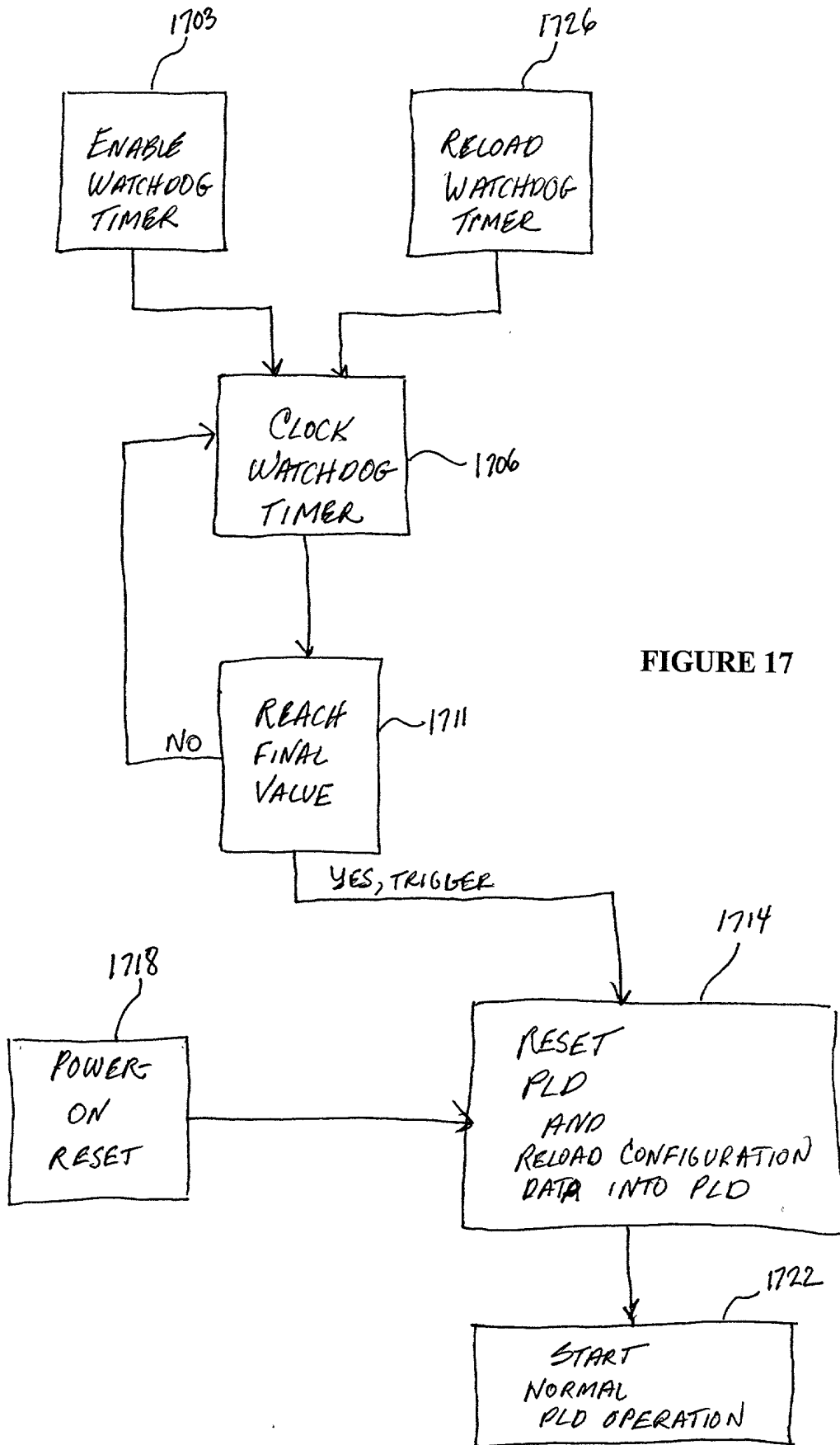


FIGURE 17